NEWS RELEASE

For more information, contact:
Larry Lapides
Vice President of Sales
(925) 519-1234
larryl@imperas.com
http://www.imperas.com

hd Lab Selects Open Virtual Platforms for SystemC Training and Model Development

OVP Fast Processor Models are Fast, Easy to Use in SystemC Environments

OXFORD, United Kingdom, October 12, 2011 – hd Lab, Inc., the leading independent design solution provider and training company in Japan, recently selected Open Virtual Platforms™ (OVP™) tools for both development of instruction accurate virtual platform models and for use in part of its SystemC training courses. Imperas, which through the OVP initiative (www.OVPworld.org) has become the de facto source for instruction accurate processor modeling and simulation, provides a native SystemC TLM-2.0 interface with all the Fast Processor Models, as well as providing a native OVP interface to the OVPsim simulator .

"For our SystemC training courses, we want the attendees to focus on building SystemC models, and how to use those models," said Hiroyasu Hasegawa, chief technology officer of hd Lab. "By using OVP Fast Processor Models, which work easily in SystemC virtual platforms, students do not have to worry about processor models, and are able to get the most out of our courses. The OVP models work well in our SystemC environment and also with other SystemC tools. We are excited to be able to expand our design service offerings in virtual platforms to our customers."

All OVP processor models are instruction accurate, and very fast, focused on enabling embedded software developers, especially those building hardware-dependent software such as firmware

and bare metal applications, to have a development environment available early to accelerate the software development cycle. OVP processor models employ a state of the art just-in-time code morphing engine to achieve the simulation speed. Virtual platforms utilizing these OVP processor models can be created with the OVP peripheral and platform models, or the processor models can be integrated into SystemC/TLM2 based virtual platforms using the native TLM2 interface available with all OVP models. The native TLM2 interface enables multiple instantiations of the processor models in a single virtual platform, just as any other component would be instantiated. The OVP simulator can also be encapsulated within the Eclipse IDE, enabling easy use for software developers.

The OVP library of Fast Processor Models includes models of the complete families of the ARMv4, ARMv5, and ARMv6 instruction set based processors, as well as models of most of the processors in the Cortex M-series and Cortex A-Series. Also included are the complete families of MIPS Technologies MIPS32 and microMIPS processors, both single and multi-core, and processor core models for the Renesas Electronics V850 family.

Virtual platforms utilizing these OVP processor models can be created with the OVP peripheral and platform models, or the processor models can be integrated into SystemC/TLM2 based virtual platforms using the TLM2 interface available with all OVP models. In addition to working with the OVP simulator, these models work with the Imperas Multiprocessor/Multicore Software Development Kit, M*SDK, which includes advanced tools for multicore software verification, analysis and debug, including key tools for software development on virtual platforms such as OS and CPU-aware tracing, profiling and code analysis.

“We are excited to have such a prominent service provider, hd Lab, as our first OVP partner in Japan,” said Larry Lapides, vice president of sales for Imperas. “We have had OVP users in

Japan since the launch of the initiative over three years ago, and with the significant growth in Imperas users in Japan, it is important to see the overall ecosystem also growing."

About Imperas (www.Imperas.com**)**

For more information about Imperas, please go to the Imperas website.

About the Open Virtual Platforms Initiative (www.OVPworld.org**)**

For more information about OVP, please go to the About OVP page on the OVP website.

Detailed quotations regarding OVP are available from http://www.ovpworld.org/quotes.

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